MASK SHOP AT THE INSTITUTE OF ELECTRONIC MATERIALS TECHNOLOGY

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Responding to recent demands from the advanced technologies of submicron lithography since 1991 ITME has used an electron-beam exposure system ZBA-20 (Carl-Zeiss-Jena) for generation of primary patterns. ZBA-20 operates on the variable shaped beam and vector scan principle and this concept compared to the Gaussian round beam principle yields a much higher productivity. Because of this advantage we successfully use ZBA-20 in two main fields of applications:

- fabrications of master masks and reticles for contact, proximity and projection lithography, especially for large-area structures, like IR and nuclear radiation detectors or SAW filters , resonators and sensors.
- direct exposure of semiconductors wafers, especially to be used in the sub-0.5-micrometer range (e.g. monolithic microwave integrated circuits).

As demonstrator from the first field of applications we manufactured microstrip detectors of very large area, that are needed in high energy physics. We recommend to our customers to order directly detector structures to avoid problems of pattern deterioration during the transfer from mask to substrate, since large areas of exactly contacting surfaces can cause problems during the separation of mask from the surface after the exposition.

Using e-beam technology we provide chromium masks with critical dimension (minimum linewidth) on level 0.5 µm and a pattern with minimum size of 0.2 µm (and better) for direct writing process. The detailed specification of both methods is shown in Table 1.

Table 1. Summary of specification.

	CHROMIUM MASKS	DIRECT WRITING ON WAFERS
substrate size	4" x 4", 5" x 5", 6" x 6"	diameters 2", 2.5", 3", 4", 5", 6"
chip size	any size up to 150 mm x 150 mm	
position resolution	0.1 µm	0.1 µm
minimum linewidth	0.5 µm	0.2 µm
overlay accuracy	≤ 0.3 µm (all levels of one set)	0.15 µm (wafers with alignment marks)
data format	DASY, CIF, D. MANN 3000, D. MANN 3600, DXF (AutoCAD)	

High resolution, short exposition time and low costs of prototyping process make direct writing method the most suitable tool for R&D works. This technique in combination with multilayer resist systems and lift-off

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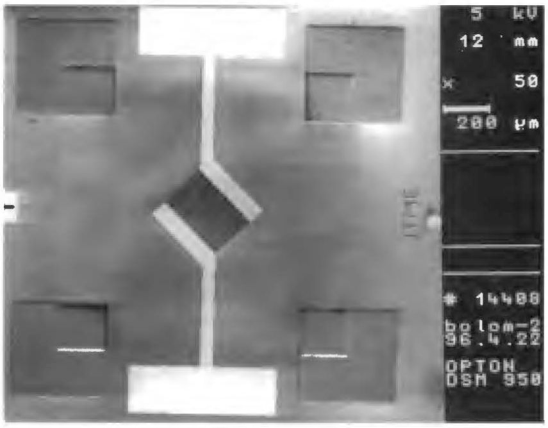

Fig. 1. A sensor of the infrared radiation - structure of the surface machined silicon bolometer.

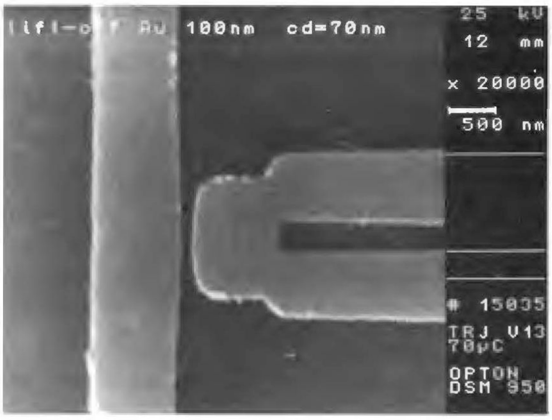

Fig. 2. Split gate 0.07 µm. Lift-off metallization Au/Cr 0.1 µm.

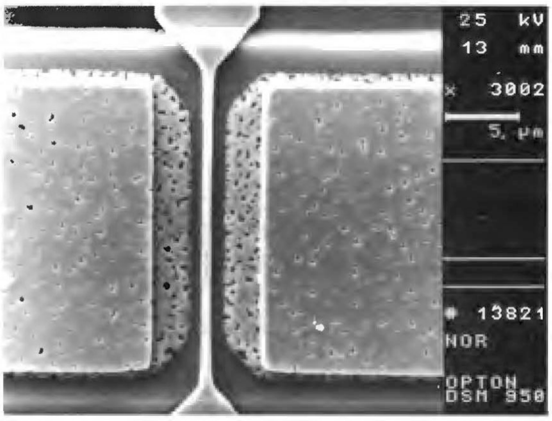

Fig. 3. Standard rectangular FET's gate 0.5 µm. Lift-off metallization Au/Cr 0.4 µm.

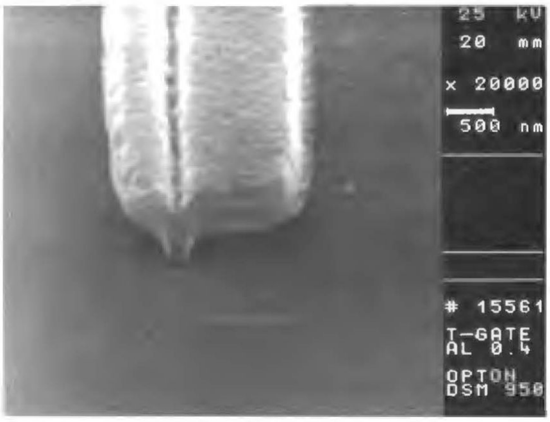

Fig. 4. The 0.2 µm foot-print T-shaped gate formed by double-layer resist system.

process enables us to produce special kind of structure, like T-shaped FET's gates, diffraction gratings or computer generated holograms.

Short biography note

Lech DOBRZAŃSKI was born in Starachowice, Poland, in 1951. He received MSc degree from Warsaw Technical University in 1974. From 1974 to 1988 he worked in Scientific & Production Center CEMI. He was involved as a leader of the technological team in a project of LEDs on GaAsP (from 1974 to 1979). The successful set up of production line was awarded in 1978. From 1980 to 1985 he was involved in a project of polish microprocessor chip. Project was completed in 1984 and awarded. From 1985 to 1988 he worked at CEMI as a designer of bipolar integrated circuits. In 1988 he joined ITME. Here he was involved in organization of a laboratory for making semiconductor devices on $A_{III}B_V$. In 1994 he received PhD degree from ITME. His research interests include modelling of technology, modelling of semiconductor devices and ICs.

Andrzej KOWALIK was born in Lublin, Poland, in 1953. He received MSc degree from Warsaw University of Technology in 1978 and began work in Laboratory of Photomask in ITME. His research is concerned with electron beam lithography.

SILICON AVALANCHE PHOTODIODES DEVELOPED AT INSTITUTE OF ELECTRON TECHNOLOGY

Iwona Węgrzecka

The paper presents the design and properties of silicon epiplanar avalanche photodiodes developed and produced at Institute of Electron Technology (ITE). These photodiodes have got the excellent parameters for the detection of very fast and very weak infrared and visible radiation (especially for the wavelength range of 800 ÷ 900 nm).

Silicon avalanche photodiodes (APDs) are the most technologically advanced from a numerous family of optical detectors such as phototransistors, photocells, p - n photodiodes, and p - i - n photodiodes. Owing to the avalanche multiplication of optically generated carriers which takes place inside the diodes structure (in the avalanche region), APDs are characterised by high internal current gain. In the modern designs (based on the p - i - n structure) the separation and transport of the optically generated carriers proceeds very fast. Since the avalanche multiplication of the carriers is also a very rapid process, the APDs are the most sensitive and fastest photodetectors. The signal to noise ratio of APDs, in the real detection circuit, is the highest among the known photodetectors and NEP values (noise equivalent of power), conditioned by this ratio, are very low. These properties make APDs indispensable in the detection of very weak signals, they perform much better than p - i - n photodiodes attached to very fast and low-noise amplifiers.

With advanced design and technology of APDs very good detector of performances can be achived:

- high quantum efficiency η_λ (photoelectric sensitivity $S_{\lambda 0}$) for unit gain (for example $\eta_\lambda = 80\%$, $S_{\lambda 0} = 0.5$ A/W at $\lambda = 850$ nm, $M = 1$),
- short rise time (a few nanoseconds),
- low operating voltage (less than 300 V),
- low dark current at given operating voltage (a few nanoampers),
- high gain at given low noise current ($M > 100$ at $I_N < 1\text{pA/Hz}^{1/2}$),
- smooth voltage - gain characteristics.

Notice: The magnitudes of most of these parameters depend on the diameter of active surface area of the photodiodes.

At Institute of Electron Technology, a family of silicon avalanche photodiodes with an active diameter from 0.3 to 3 mm has been developed and produced. These photodiodes are optimised for the wavelength range of 800 ÷ 900 nm. They have got an $n^+ - p - \pi - p^+$ epiplanar structure with an n - type guard ring, a p - type channel stopper and an $n^+ - p$ hyper-abrupt junction of the avalanche region.

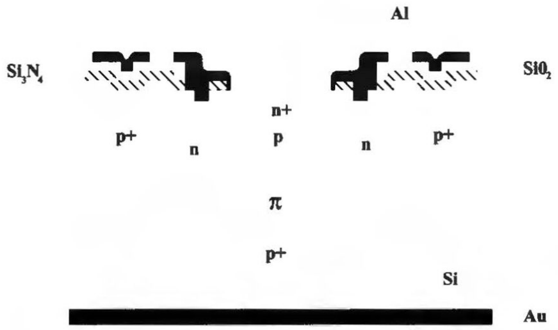

Fig. 1. Cross-section of the avalanche photodiode structure developed in ITE.

The schematic cross section of these photodiodes is shown in the Fig. 1. The initial material is a silicon wafer with a p - type epitaxial layer ($\rho_\pi = 200 \div 250\ \Omega$cm, $x_\pi = 30 \div 35\ \mu$m) grown on a p^+ - type, <111> orientated substrate. The n - type guard ring is provided by phosphorus pre-diffusion from $POCl_3$ source, followed by re-diffusion that takes place during thermal treatment of the active area ($N_S = 5\times10^{20}$ cm^{-3}, $x_j = 7\ \mu$m). The p - type channel stopper is made by implanting and then re-diffusing boron (re-diffusing is common for p^+ and p areas), $N_S > 10^{18}$cm^{-3}.

The photodiode active area (photosensitive, avalanche), covered with a 150 nm thick SiO_2 antireflection layer, constitutes the central area with the n^+ - p hyper-abrupt junction obtained by the arsenic diffusion from the amorphous silicon (doped with As during the deposition process) to the p - type region which was previously obtained by boron implantation and then boron re-diffusion.

The n^+ - p junction parameters for the designed APD structures, should attain values as follows:

- junction depth	$x_j \cong 0.4\ \mu$m,
- arsenic surface concentration	$N_S \cong 6\times10^{19}$ cm^{-3},
- boron surface concentration	optimum,
- p layer thickness	$x_p \cong 4.5\ \mu$m.

The photodiode structure is covered with a Si_3N_4 layer (~100 nm). An ohmic contact to the n - type region is made of aluminium and to the p - type substrate of gold.

A dopant distribution in an active region of APD is shown in Fig. 2. An optimal electric field distribution in a structure of APD at operating voltage is shown in Fig. 3.

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